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(SFW)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: **Xie, et al.**

Serial No.: 10/673,597

Filed: September 29, 2003

For: **Slurry-Less Polishing for Removal of
Excess Interconnect Material During
Fabrication of a Silicon Integrated
Circuit**

Art Unit: 2812

Examiner: Gurley, Lynne Ann

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This is an Appeal from the Examiner's Final Rejection of claims 31, 33-34, and 36-40. The Final Rejection issued on December 30, 2005. The Notice of Appeal was filed in the U.S. Patent and Trademark Office on March 27, 2006.

05/26/2006 CCHAU1 00000077 10673597

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REAL PARTY IN INTEREST

The real party in interest is Advanced Micro Devices, Inc.

RELATED APPEALS AND INTERFERENCES

There are no related Appeals or Interferences.

STATUS OF CLAIMS

Claims 31, 33-34, and 36-40 are pending, and claims 1-30, 32, and 35 were canceled in previous amendments. Claims 31, 33-34, and 36-40 have been finally rejected in a Final Rejection dated December 30, 2005. This Appeal is directed to the rejection of claims 31, 33-34, and 36-40. Claims 31, 33-34, and 36-40 appear in an Appendix to this Appeal Brief.

STATUS OF AMENDMENTS

No claim amendments were submitted in the response to or subsequent to the Final Rejection dated December 30, 2005.

SUMMARY OF CLAIMED SUBJECT MATTER

A. Claim 31

Independent claim 31 defines a method for removing excess interconnect material during fabrication of a silicon integrated circuit, where the method comprises dispensing

a slurry (e.g., step 24 in Figure 2a) using a dispenser (e.g., dispenser 212 in Figure 2b) including abrasive particles and chemical on a sample silicon integrated circuit (e.g., sample 206 in Figure 2b). *See, e.g., the present application, page 4, line 26 through page 5, line 5.*

The sample is polished with the slurry and a polishing pad (e.g., polishing pad 200 in Figure 2b) having a number of pits (e.g., pits 201 in Figure 2b). During this process the abrasive particles and chemical become embedded into the pits of the polishing pad. *See, e.g., the present application, page 5, lines 6-8.* After detecting an endpoint in the step of polishing the sample with the slurry, the endpoint being detected based on a thickness of the excess interconnect material, the dispensing of the slurry is halted (e.g., step 26 in Figure 2a). Then, a slurry-less polishing is utilized for fine removal of the remaining excess materials (e.g., step 26 in Figure 2a). *See, e.g., the present application, page 5, lines 16-18.*

GROUND OF REJECTION TO BE REVIEWED ON APPEAL

- A. Claims 31, 33-34, and 36-40 under 35 USC §102(e) as being anticipated by US published application number 2003/0162399 to Singh (hereinafter “Singh”).
- B. Claims 33-34 and 38 under 35 USC §103(a) as being unpatentable over Singh in view of U.S. Patent No. 5,441,598 to Yu (hereinafter “Yu”).

ARGUMENT

A. Rejection of Claims 31, 33-34, and 36-40 Under 35 USC § 102(e)

The Examiner has rejected claims 31, 33-34, and 36-40 under 35 USC §102(e) as being anticipated by US published application number 2003/0162399 to Singh (hereinafter “Singh”). The present invention, as defined by independent claim 31 is directed to, among other things, reducing dishing in metal features during CMP process. The present invention, as defined by independent claim 31 requires that, after passage of a first time period, the flow rate of the slurry during a second time period be reduced and in fact be stopped so that during the second time period only a polishing action, with no slurry flow, would occur. As such, independent claim 31 requires “reducing said dispensing of said slurry after said polishing for a first period of time, wherein said dispensing of said slurry is reduced to a stop” followed by “polishing said sample using said polishing pad for a second period of time to remove said excess interconnect material.” Moreover, independent claim 31 requires the reduction in dispensing the slurry to occur after detection of an endpoint of the polishing step based on a thickness of the excess interconnect material.

In contrast, Singh discloses chemical mechanical polishing of a structure with one or more metal based films and at least one underlying dielectric film with at least one selective adsorption additive, such as a surfactant or a polymer. The metal film does not substantially adsorb the selective adsorption additive surfactant, while dielectric film substantially adsorbs the selective adsorption additive. A number of composite particles

are added, such as inorganic cores surrounded by the selective adsorption additive. Singh also discloses a method for polishing a metal film and an underlying dielectric film including polishing during a first time interval using a first slurry composition and polishing during a second time interval with a second slurry composition, wherein a selectivity ratio for metal/dielectric polishing using the first slurry composition to the metal/dielectric selectivity using the second slurry composition is fixed.

However, Singh does not disclose stopping the flow rate of the slurry after passage of a first time period, and performing only a polishing action, with no slurry flow. Further, Singh does not disclose that the reduction in dispensing the slurry occurs after detection of an endpoint of the polishing step based on a thickness of the excess interconnect material.

The Examiner has pointed to paragraph 0143 of Singh as disclosing that the Singh method is “selective to the metal materials using optical sensors (which inherently takes into consideration the endpoint detection and thickness of the interconnect materials).” Final Office Action of December 30, 2005, the last sentence on Page 3.

However, paragraph 0143 of Singh states in its entirety:

“FIG. 9 shows an apparatus 900 designed to feed the interval and continuous slurry for metal polishing. Mixing of the interval slurry 902 and continuous slurry 904 can take place in a mixing tank 910 before being supplied to the CMP tool. Alternatively, the continuous and interval slurries can be mixed on the polishing tool at the point of use (on polishing pad 920). *An optical or a frictional based sensor (not shown) can be used to*

monitor the surface condition of the wafer. Other types of sensing mechanisms based on acoustic, vibration and other techniques can also be used. The interval slurry is typically added when the metal overlayer has been substantially removed from the surface. The apparatus can be used to polish a wide variety of electrically conducting materials including, refractory materials and noble metals, as well as related electrically conducting compounds and mixtures.” Page 13 of Singh, paragraph 0143 (emphasis added).

In contrast, the invention discloses and claims that the reduction in dispensing the slurry occurs after detection of an endpoint of the polishing step based on a thickness of the excess interconnect material. None of these elements is disclosed by paragraph 0143 of Singh: Singh merely suggests that “[a]n optical or a frictional based sensor” be used to monitor the surface condition of the wafer and not the thickness of material. Furthermore, Singh does not perform such sensing to detect an endpoint of the polishing step or to reduce the dispensing of the slurry. As such, Singh does not disclose or suggest the invention claimed by independent claim 31. Thus, dependent claims 33-34 and 36-40 are also patentably distinguishable over Singh for at least the reasons discussed above and for added limitations of each dependent claim.

B. Rejection of Claims 33-34 and 38 Under 35 USC § 103(a)

The Examiner has rejected claim 33-34 and 38 under 35 USC §103(a) as being unpatentable over Singh in view of U.S. Patent No. 5,441,598 to Yu (hereinafter “Yu”). As discussed above, independent claim 31 is patentably distinguishable over Singh.

Thus, dependent claims 34 and 38 are also patentably distinguishable over Singh, or any combination of Singh and Yu, for at least the reasons discussed above and for the added limitations in each dependent claim.

CONCLUSION

Based on the foregoing reasons, Applicant respectfully submits that independent claim 31 and its dependent claims 33-34, and 36-40 are patentable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early notice of allowance directed to claims 31, 33-34, and 36-40 remaining in the present application is respectfully requested.

This Appeal Brief is submitted herewith with an Appendix of the appealed claims and the requisite fee for filing the Appeal Brief.

Respectfully Submitted,
FARJAMI & FARJAMI LLP

Date: 5/23/06



Michael Farjami, Esq.
Reg. No. 38, 135

FARJAMI & FARJAMI LLP
26522 La Alameda Ave., Suite 360
Mission Viejo, California 92691
Telephone: (949) 282-1000
Facsimile: (949) 282-1002

CERTIFICATE OF MAILING

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Date of Deposit: 5/23/06

Christina Carter
Name of Person Mailing Paper and/or Fee

Christina Carter 5/23/06
Signature Date

APPENDIX OF CLAIMS ON APPEAL

Claim 31: A silicon integrated circuit fabricated using a method of removing excess interconnect material during fabrication of said silicon integrated circuit, said method of removing comprising the steps of:

dispensing a slurry including abrasive particles and chemical on a sample having said excess interconnect material;

polishing said sample with said slurry, using a polishing pad having a plurality of pits, to remove said excess interconnect material, wherein said abrasive particles and chemical become embedded into said plurality of pits of said polishing pad;

reducing said dispensing of said slurry after said polishing for a first period of time, wherein said dispensing of said slurry is reduced to a stop, said step of reducing occurring after detecting an endpoint of said step of polishing said sample with said slurry, based on a thickness of said excess interconnect material; and

polishing said sample using said polishing pad for a second period of time to remove said excess interconnect material.

Claim 33: The silicon integrated circuit of claim 31, wherein said silicon integrated circuit includes a metal gate fabricated with Atomic Layer Deposition (ALD) and said excess interconnect material is copper.

Claim 34: The silicon integrated circuit of claim 33, wherein said ALD includes Ta.

Claim 36: The silicon integrated circuit of claim 31, wherein said thickness of said excess interconnect material is determined based on optical reflectivity.

Claim 37: The silicon integrated circuit of claim 31, said excess interconnect material is copper.

Claim 38: The silicon integrated circuit of claim 31, wherein said plurality of pits are created by abrading a polishing surface of said polishing pad with an abrasive disc.

Claim 39: The silicon integrated circuit of claim 31, wherein said steps of polishing are performed at a pressure of about 1.5 psi.

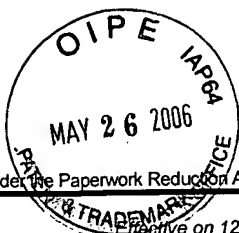
Claim 40: The silicon integrated circuit of claim 31, wherein said steps of polishing are performed at a pressure of about 2.7 psi.

EVIDENCE APPENDIX

(NONE)

RELATED PROCEEDINGS APPENDIX

(NONE)



PTO/SB/17 (12-04)

Approved for use through 07/31/2006. OMB 0651-0032

U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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FEE TRANSMITTAL For FY 2005 <input type="checkbox"/> Applicant Claims small entity status. See 37 CFR 1.27		Complete if Known		
		Application Number	10/673,597	
		Filing Date	09/29/2003	
		First Named Inventor	Xie	
		Examiner Name	Gurley, Lynne Ann	
TOTAL AMOUNT OF PAYMENT		\$500.00	Attorney Docket No.	0180227

METHOD OF PAYMENT (check all that apply)

☐ Check ☒ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 50-0731 Deposit Account Name: Farjami & Farjami LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☐ Charges fee(s) indicated below, except for the filing fee

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FEE CALCULATION**1. BASIC FILING, SEARCH, AND EXAMINATION FEES**

Application Type	FILING FEES		SEARCH FEES		EXAMINATION FEES		Fees Paid (\$)
	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee (\$)	Small Entity Fee (\$)
Each claim over 20 or, for Reissues, each claim over 20 and more than in the original patent	50	25
Each independent claim over 3 or, for Reissues, each independent claim more than in the original patent	200	100
Multiple dependent claims	360	180
Total Claims	Extra Claims	Fee (\$)
- 20 or HP = 0	x	\$50.00
HP = highest number of total claims paid for, if greater than 20		
Indep. Claims	Extra Claims	Fee (\$)
- 3 or HP = 0	x	\$200.00
HP = highest number of independent claims paid for, if greater than 3		

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41 (a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee (\$)	Fee Paid (\$)
- 100 = 0	/ 50 = 0	(round up to a whole number) x	\$250.00	\$ 0.00

4. OTHER FEE(S)

Non-English Specification, \$130 fee (no small entity discount)

Other: Filing a brief in support of an appeal

\$500.00

SUBMITTED BY

Signature		Registration No. (Attorney/Agent)	38135	Telephone	(949) 282-1000
Name (Print/Type)	Michael Farjami, Esq.	Date	5/23/06		

This collection of information is required by 37 CFR 1.136. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.